CLAIMS

We Claim:

1. A method for making an embedded semiconductor memory device comprising:

forming one or more diffusion bit line regions in a semiconductor substrate; then

thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions; and then

forming an intermediate dielectric layer over the bottom oxide layer and the bit line oxide regions.

2. The method of Claim 1, wherein the intermediate dielectric layer comprises silicon nitride.

3. The method of Claim 1, further comprising depositing a top dielectric layer over the intermediate dielectric layer using a chemical vapor deposition process.

4. The method of Claim 3, wherein the top dielectric layer is formed by depositing high-temperature silicon oxide.

5. The method of Claim 3, wherein the top dielectric layer is a high dielectric material, having a dielectric constant equal to 4 or greater.

6. The method of Claim 3, wherein the top dielectric layer is deposited at a temperature of about 750 to 850°C.

7. The method of Claim 1, further comprising implanting CMOS well regions through the intermediate dielectric layer and the bottom oxide layer in a first region of the semiconductor substrate.

8. The method of Claim 7, further comprising:

removing the intermediate dielectric layer and the bottom oxide layer in the first region of the semiconductor substrate; and then

depositing a top dielectric layer over the nitride layer and the first region of the semiconductor substrate using a chemical vapor deposition process.

9. The method of Claim 8, further comprising fabricating one or more high-voltage transistors in the first region of the semiconductor substrate, wherein the high-voltage transistors use the top dielectric layer as a gate dielectric layer.

10. The method of Claim 8, further comprising forming a sacrificial oxide layer over the first region of the semiconductor substrate after removing the intermediate dielectric layer and the bottom oxide layer, but before depositing the top dielectric layer

11. The method of Claim 9, further comprising fabricating one or more low-voltage transistors in the first region of the semiconductor substrate, wherein each of the

low voltage logic transistors have a gate dielectric layer thinner than the top dielectric layer.

12. The method of Claim 1, further comprising forming shallow trench isolation regions in the semiconductor substrate prior forming the one or more diffusion bit line regions in the semiconductor substrate.

13. The method of Claim 1, wherein each of the bit line oxide regions has a thickness that is about 1.5 to 3 times larger than a thickness of the bottom oxide layer.

14. The method of Claim 1, wherein each bit line oxide region has a thickness in the range of about 50 to 150 Angstroms.

15. The method of Claim 1, further comprising:

forming a conductive layer over the top dielectric layer;

patterning the conductive layer to define a plurality of word lines that extend over the bit line oxide regions and the bottom oxide layer; and

removing the top dielectric layer and intermediate dielectric layer located between the plurality of word lines.